

PHASE CONTROL THYRISTOR

AT940

Repetitive voltage up to **2900 V**
Mean on-state current **4687 A**
Surge current **75 kA**

FINAL SPECIFICATION

Feb. 17 - Issue: 6

Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	2900	V
V _{RSM}	Non-repetitive peak reverse voltage		125	3000	V
V _{DRM}	Repetitive peak off-state voltage		125	2900	V
I _{RRM}	Repetitive peak reverse current	V=V _{RRM}	125	300	mA
I _{DRM}	Repetitive peak off-state current	V=V _{DRM}	125	300	mA
CONDUCTING					
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		4687	A
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		3638	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	125	75,0	kA
I ² t	I ² t	without reverse voltage		28125 x1E3	A ² s
V _T	On-state voltage	On-state current = 7500 A	25	1,55	V
V _{T(TO)}	Threshold voltage		125	1,00	V
r _T	On-state slope resistance		125	0,070	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% V _{DRM} , gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V _{DRM}	125	1000	V/μs
t _d	Gate controlled delay time, typical	V _D =100V, gate source 10V, 10 ohm, tr=5 μs	25		μs
t _q	Circuit commutated turn-off time, typical	dv/dt = 20 V/μs linear up to 75% V _{DRM}		500	μs
Q _{RR}	Reverse recovery charge	di/dt=-20 A/μs, I _s = 2150 A	125		μC
I _{RR}	Peak reverse recovery current	V _R = 50 V			A
I _H	Holding current, typical	V _D =5V, gate open circuit	25	500	mA
I _L	Latching current, typical	V _D =12V, tp=30μs	25	1000	mA
GATE					
V _{GT}	Gate trigger voltage	V _D =12V	25	3,5	V
I _{GT}	Gate trigger current	V _D =12V	25	400	mA
V _{GD}	Non-trigger gate voltage, min.	V _D =V _{DRM}	125	0,25	V
V _{FGM}	Peak gate voltage (forward)			10	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			10	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			3	W
MOUNTING					
R _{th(j-c)}	Thermal impedance, DC	Junction to case, double side cooled		6,0	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, double side cooled		1,5	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
F	Mounting force			80.0 / 100.0	kN
	Mass			3000	g

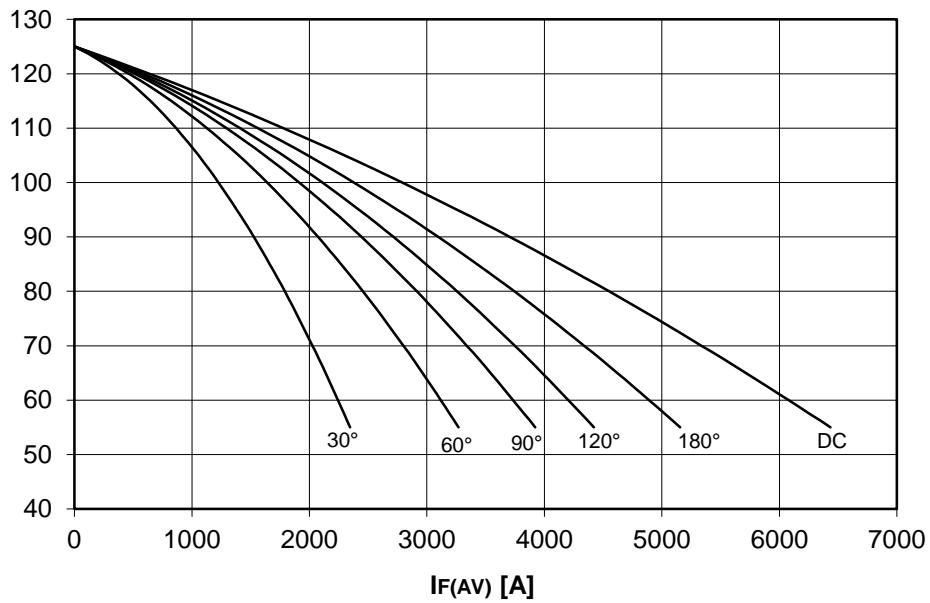
ORDERING INFORMATION : AT940 S 29

standard specification VDRM&VRRM/100

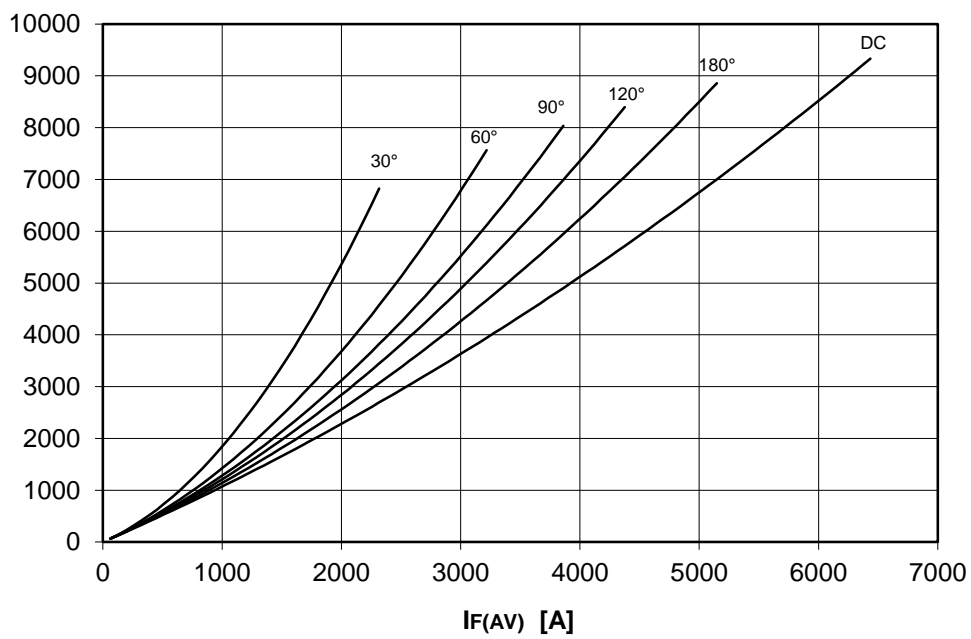
DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



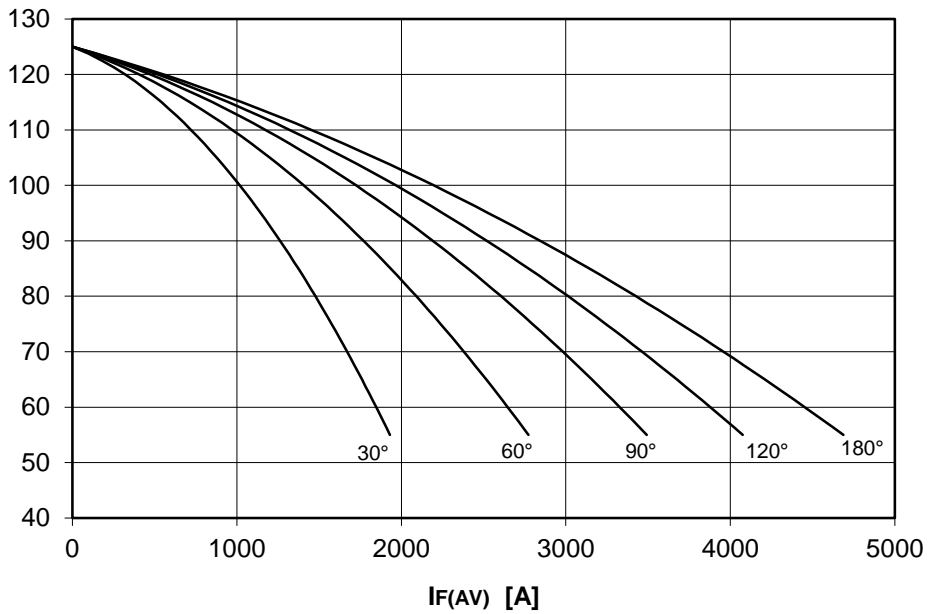
PF(AV) [W]



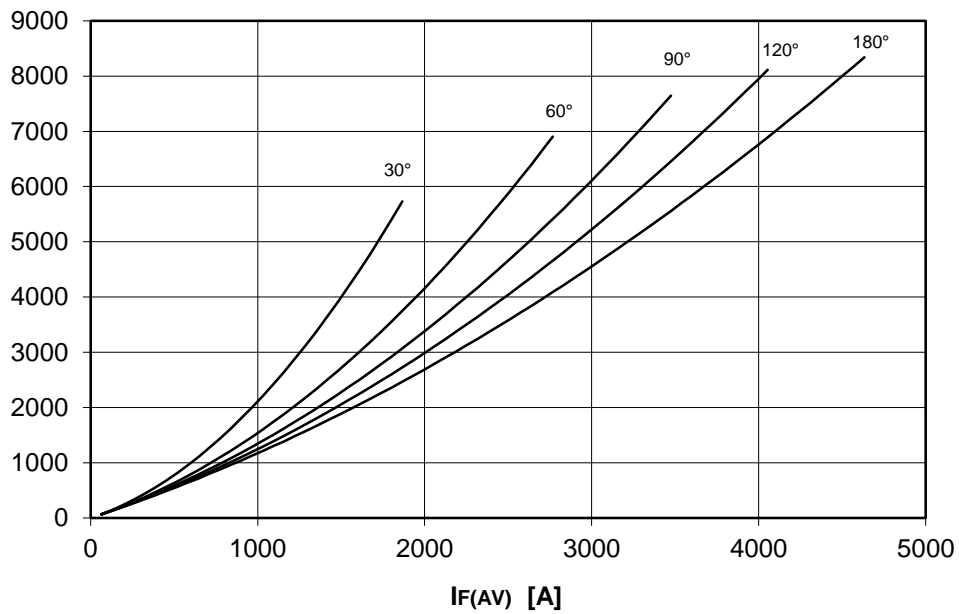
DISSIPATION CHARACTERISTICS

SINE WAVE

Th [°C]

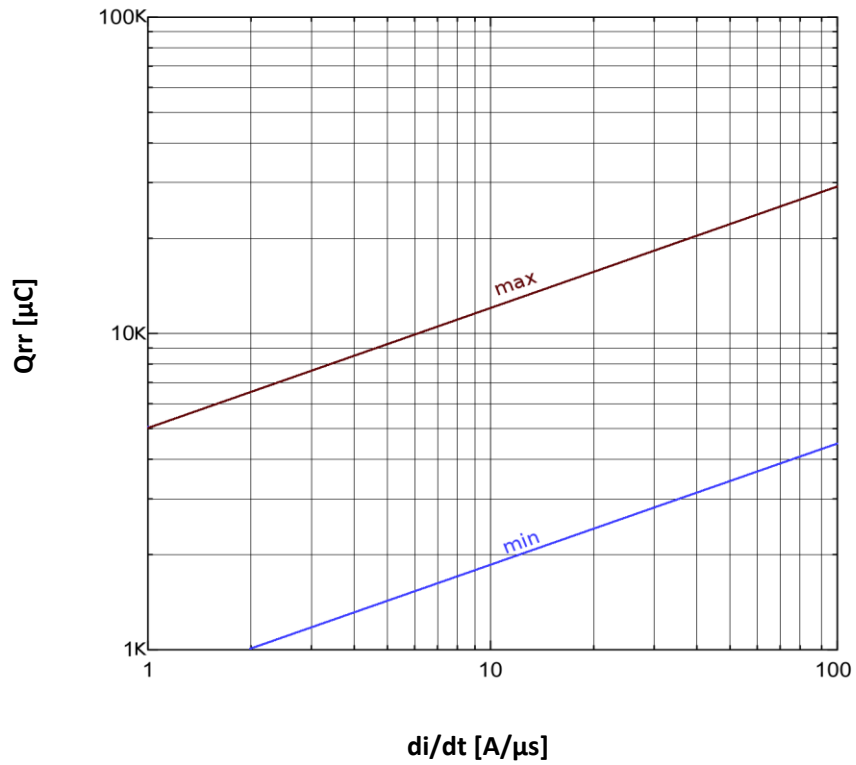


PF(AV) [W]



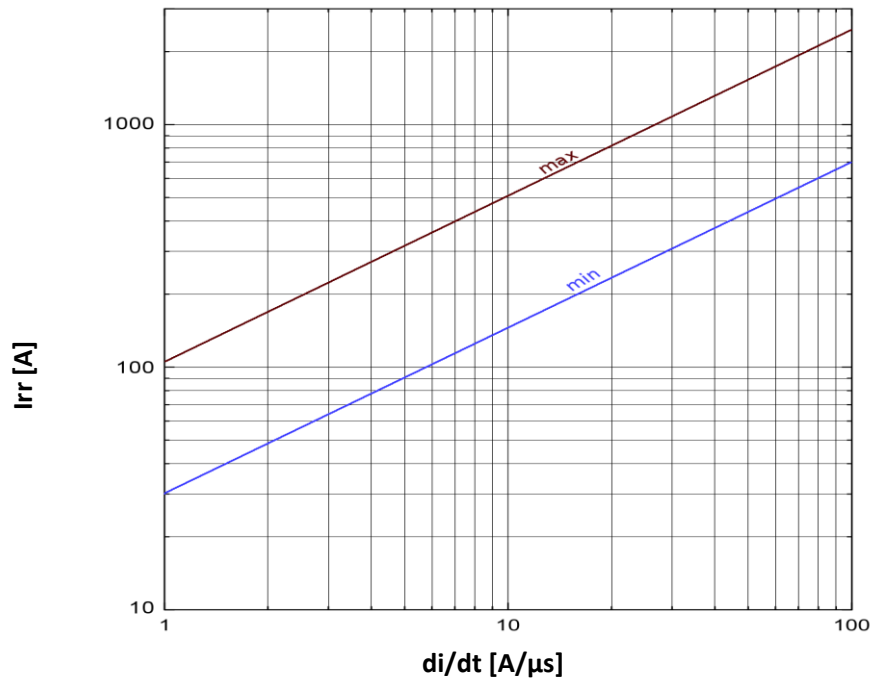
REVERSE RECOVERY CHARGE

$T_j = 125^\circ\text{C} - I_T = 3000\text{ A}$

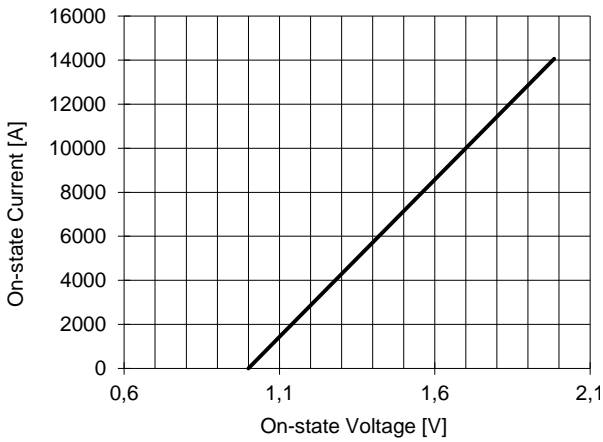


REVERSE RECOVERY CURRENT

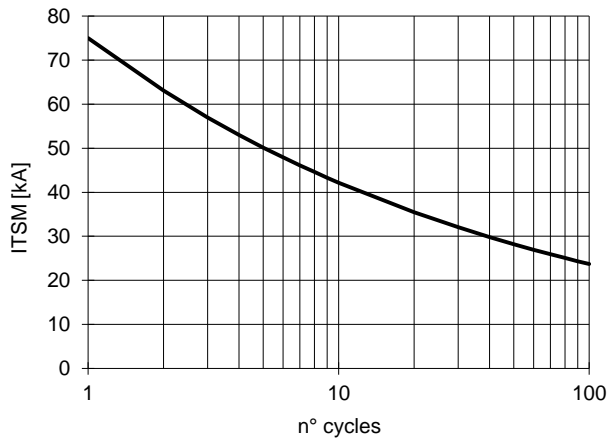
$T_j = 125^\circ\text{C} - I_T = 3000\text{ A}$



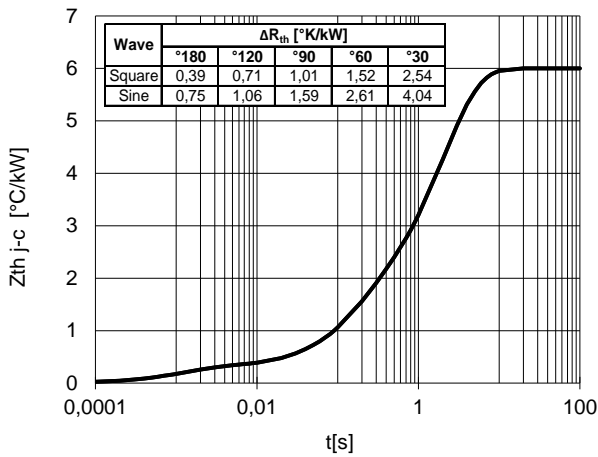
ON-STATE CHARACTERISTIC
T_j = 125 °C



SURGE CHARACTERISTIC
T_j = 125 °C

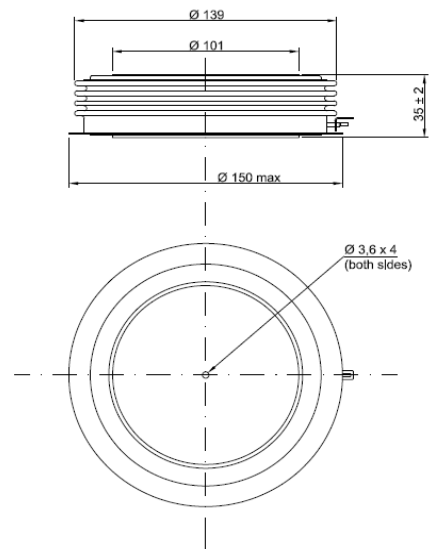


TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



$$Z_{th\ j-c}(t) = \sum_{i=1}^n A_i * \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

i	1	2	3	4
A _i [°C/kW]	2,738	1,779	1,186	0,297
τ _i [s]	2,4	1,70	0,16	0,001



Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

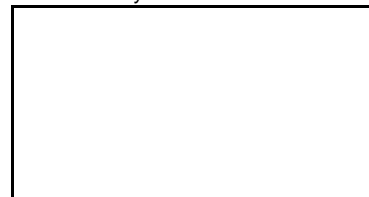
Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.

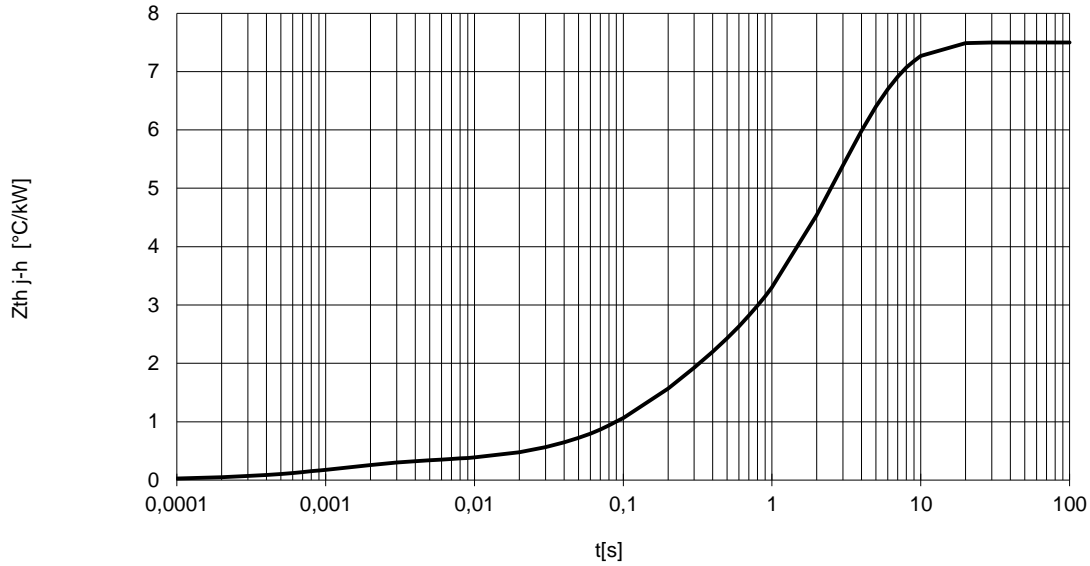
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



$$Z_{th\ j-h}(t) = \sum_{i=1}^n A_i * \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

i	1	2	3	4
A _i [°C/kW]	4,320	1,701	1,183	0,296
τ _i [s]	3,400	1,800	0,160	0,001

Note:

This Z_{th_j-h}(t) curve takes into account of a contact thermal resistance value R_{th_c-h} = 1,5 °C/kW.

Mounting recommendations must be followed in order to match the specified contact thermal resistance value.