High Voltage Thyristor \ Diode Module

V_{RRM}	=	2x 2200 V
I_{TAV}	=	180 A
V_T	=	1.18 V

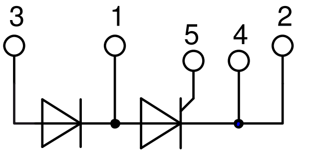
Phase leg

Part number

MCNA180PD2200YB

Backside: isolated

E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

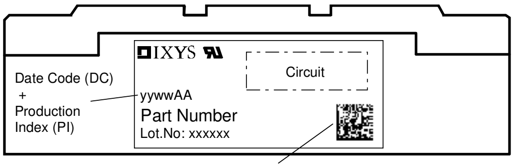
Package: Y4

- Isolation Voltage: 4800 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

Rectifier				Ratings			
Symbol	**Definition**	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
$V_{RSM/DSM}$	*max. non-repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			2300	V
$V_{RRM/DRM}$	*max. repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			2200	V
$I_{R/D}$	*reverse current, drain current*	$V_{R/D}$ = 2200 V	T_{VJ} = 25°C			400	µA
		$V_{R/D}$ = 2200 V	T_{VJ} = 125°C			30	mA
V_T	*forward voltage drop*	I_T = 180 A	T_{VJ} = 25°C			1.24	V
		I_T = 360 A				1.49	V
		I_T = 180 A	T_{VJ} = 125°C			1.18	V
		I_T = 360 A				1.51	V
I_{TAV}	*average forward current*	T_C = 85°C	T_{VJ} = 140°C			180	A
$I_{T(RMS)}$	*RMS forward current*	180° sine				280	A
V_{T0}	*threshold voltage*	*for power loss calculation only*	T_{VJ} = 140°C			0.85	V
r_T	*slope resistance*					1.8	mΩ
R_{thJC}	*thermal resistance junction to case*					0.17	K/W
R_{thCH}	*thermal resistance case to heatsink*				0.090		K/W
P_{tot}	*total power dissipation*		T_C = 25°C			675	W
I_{TSM}	*max. forward surge current*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			5.40	kA
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			5.83	kA
		t = 10 ms; (50 Hz), sine	T_{VJ} = 140°C			4.59	kA
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			4.96	kA
I^2t	*value for fusing*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			145.8	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			141.4	kA²s
		t = 10 ms; (50 Hz), sine	T_{VJ} = 140°C			105.3	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			102.1	kA²s
C_J	*junction capacitance*	V_R = 700 V f = 1 MHz	T_{VJ} = 25°C		146		pF
P_{GM}	*max. gate power dissipation*	t_P = 30 µs	T_C = 140°C			120	W
		t_P = 300 µs				60	W
P_{GAV}	*average gate power dissipation*					8	W
$(di/dt)_{cr}$	*critical rate of rise of current*	T_{VJ} = 140°C; f = 50 Hz	repetitive, I_T = 540 A			150	A/µs
		t_P = 200 µs; di_G/dt = 0.5 A/µs;					
		I_G = 0.5 A; V = ⅔ V_{DRM}	non-repet., I_T = 180 A			500	A/µs
$(dv/dt)_{cr}$	*critical rate of rise of voltage*	V = ⅔ V_{DRM}	T_{VJ} = 140°C			1000	V/µs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{GT}	*gate trigger voltage*	V_D = 6 V	T_{VJ} = 25°C			2	V
			T_{VJ} = -40°C			2.6	V
I_{GT}	*gate trigger current*	V_D = 6 V	T_{VJ} = 25°C			150	mA
			T_{VJ} = -40°C			200	mA
V_{GD}	*gate non-trigger voltage*	V_D = ⅔ V_{DRM}	T_{VJ} = 140°C			0.2	V
I_{GD}	*gate non-trigger current*					10	mA
I_L	*latching current*	t_p = 30 µs	T_{VJ} = 25°C			200	mA
		I_G = 0.45 A; di_G/dt = 0.45 A/µs					
I_H	*holding current*	V_D = 6 V R_{GK} = ∞	T_{VJ} = 25°C			200	mA
t_{gd}	*gate controlled delay time*	V_D = ½ V_{DRM}	T_{VJ} = 25°C			2	µs
		I_G = 0.5 A; di_G/dt = 0.5 A/µs					
t_q	*turn-off time*	V_R = 100 V; I_T = 180 A; V = ⅔ V_{DRM}	T_{VJ} = 125 °C		200		µs
		di/dt = 10 A/µs dv/dt = 20 V/µs t_p = 200 µs					

Package Y4

Symbol	Definition	Conditions			min.	typ.	max.	Unit
I_{RMS}	*RMS current*	per terminal					300	A
T_{VJ}	*virtual junction temperature*				-40		140	°C
T_{op}	*operation temperature*				-40		125	°C
T_{stg}	*storage temperature*				-40		125	°C
Weight						150		g
M_D	*mounting torque*				2.25		2.75	Nm
M_T	*terminal torque*				4.5		5.5	Nm
$d_{Spp/App}$	*creepage distance on surface | striking distance through air*		*terminal to terminal*	14.0	10.0			mm
$d_{Spb/Apb}$			*terminal to backside*	16.0	16.0			mm
V_{ISOL}	*isolation voltage*	t = 1 second	50/60 Hz, RMS; $I_{ISOL} \le 1$ mA		4800			V
		t = 1 minute			4000			V



Data Matrix: *part no.* (1-19), DC + *PI* (20-25), *lot.no.#* (26-31), *blank* (32), *serial no.#* (33-36)

Part description

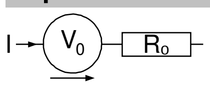
- M = Module
- C = Thyristor (SCR)
- N = High Voltage Thyristor
- A = (>= 2000V)
- 180 = Current Rating [A]
- PD = Phase leg
- 2200 = Reverse Voltage [V]
- YB = Y4-M6

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCNA180PD2200YB	MCNA180PD2200YB	Box	6	520502

Similar Part	Package	Voltage class
MCNA150PD2200YB	Y4-M6	2200
MCNA220PD2200YB	Y4-M6	2200

Equivalent Circuits for Simulation

** on die level* $T_{VJ} = 140\,°C$

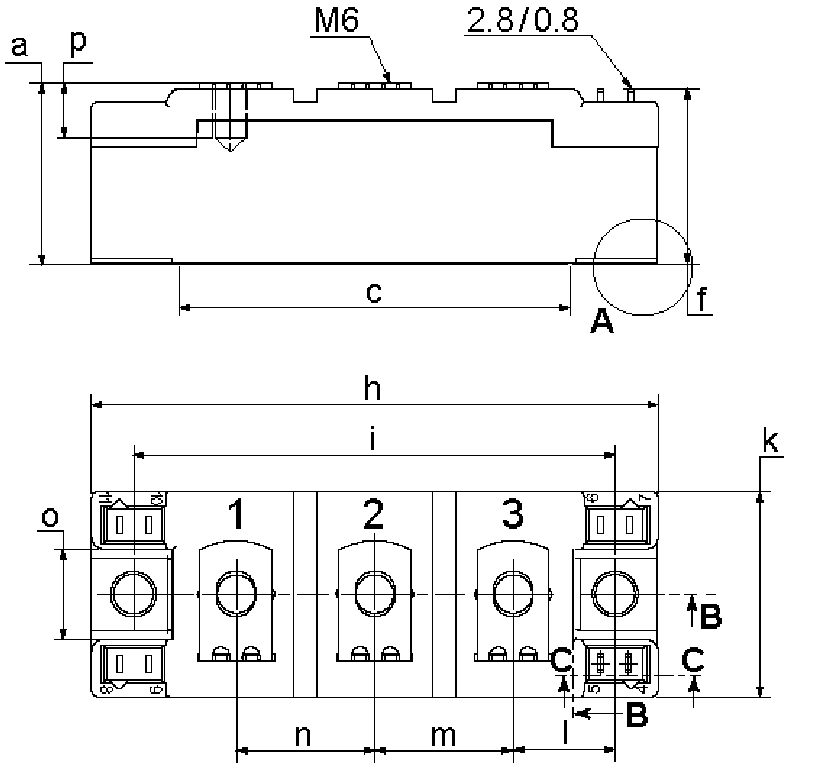


Thyristor

$V_{0\,max}$	*threshold voltage*	0.85	V
$R_{0\,max}$	*slope resistance **	1.18	mΩ

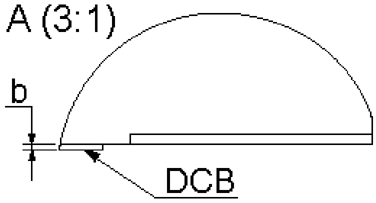
IXYS reserves the right to change limits, conditions and dimensions. Data according to IEC 60747and per semiconductor unless otherwise specified 20160718a

Outlines Y4

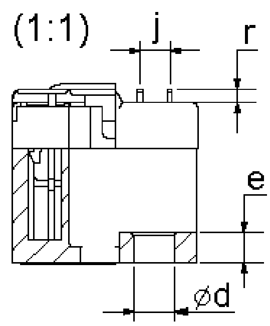


Dim.	MIN [mm]	MAX [mm]	MIN [inch]	MAX [inch]
a	30.0	30.6	1.181	1.205
b	typ. 0.25		typ. 0.010	
c	64.0	65.0	2.520	2.559
d	6.5	7.0	0.256	0.275
e	4.9	5.1	0.193	0.201
f	28.6	29.2	1.126	1.150
g	7.3	7.7	0.287	0.303
h	93.5	94.5	3.681	3.720
i	79.5	80.5	3.130	3.169
j	4.8	5.2	0.189	0.205
k	33.4	34.0	1.315	1.339
l	16.7	17.3	0.657	0.681
m	22.7	23.3	0.894	0.917
n	22.7	23.3	0.894	0.917
o	14.0	15.0	0.551	0.591
p	typ. 10.5		typ. 0.413	
r	1.8	2.4	0.071	0.041

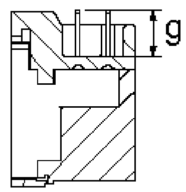
A (3:1)

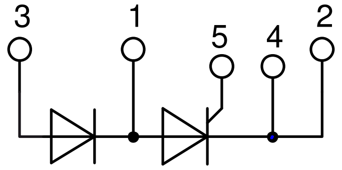


B-B (1:1)



C-C (1:1)





Thyristor

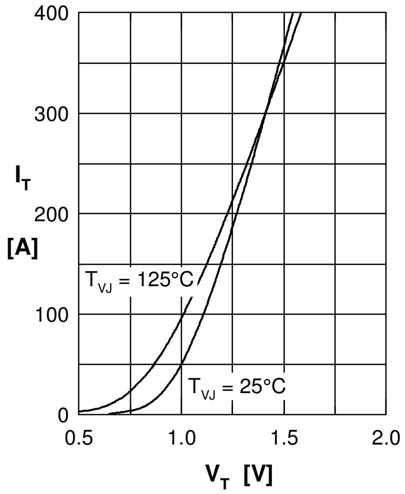


Fig. 1 Forward characteristics

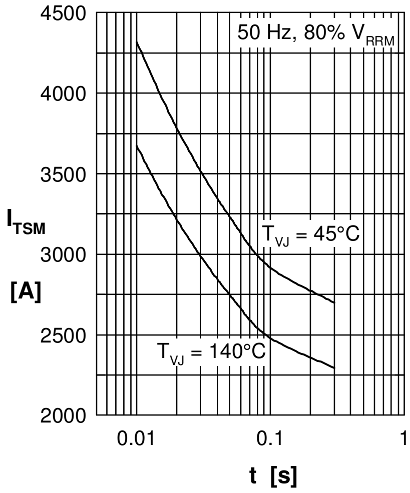


Fig. 2 Surge overload current
I_{TSM}: crest value, t: duration

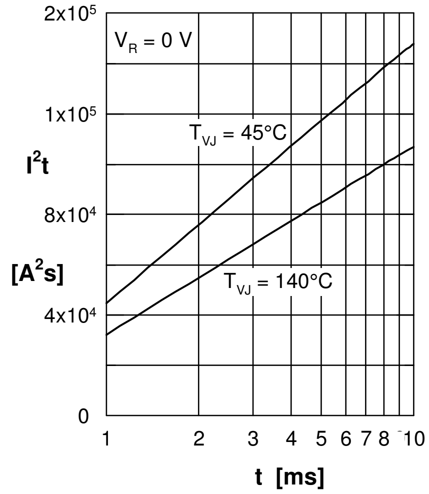


Fig. 3 I^2t versus time (1-10 s)

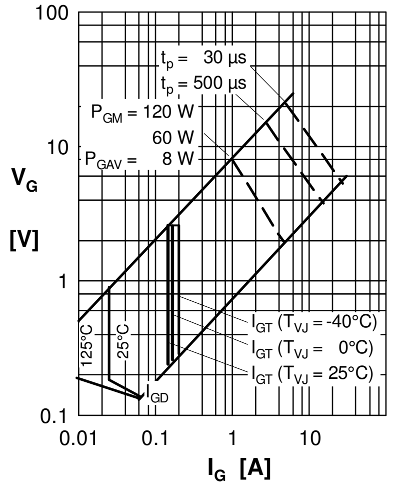


Fig. 4 Gate voltage & gate current

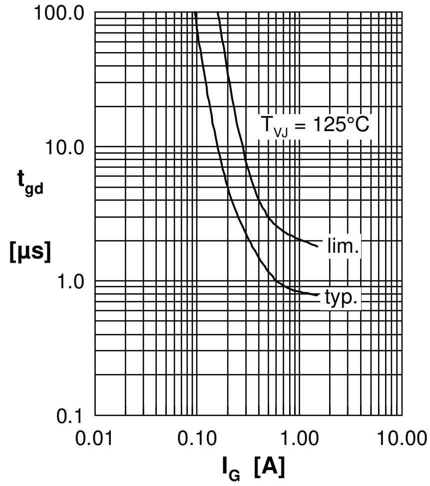


Fig. 5 Gate controlled delay time t_{gd}

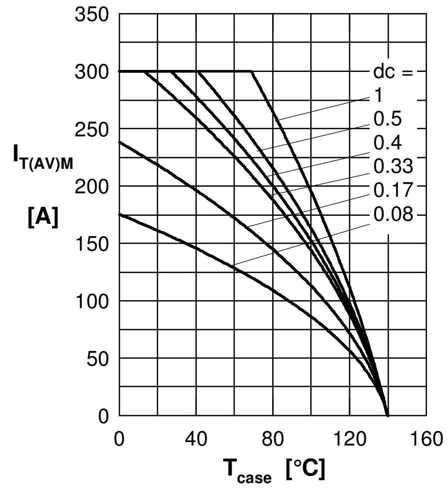


Fig. 6 Max. forward current at case temperature

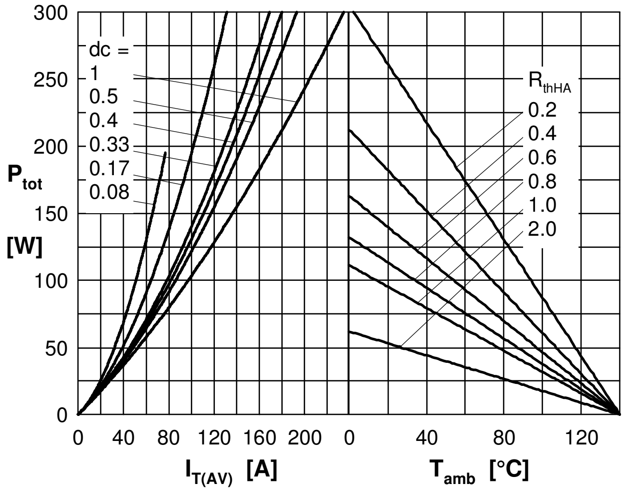


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature

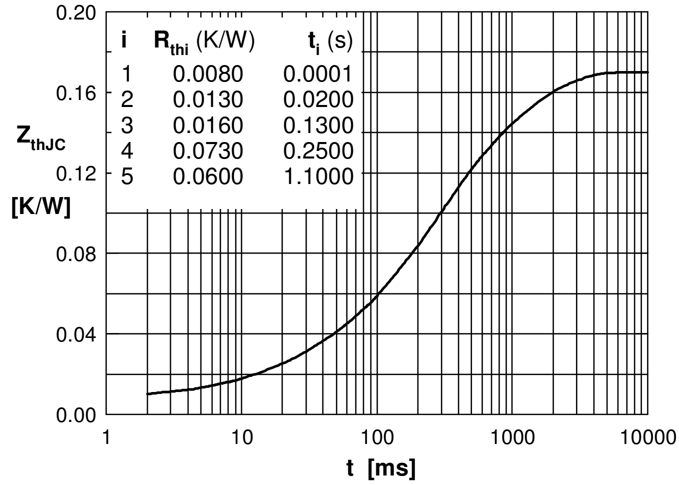


Fig. 8 Transient thermal impedance junction to case